## **CLAIMS**

## What is claimed is:

2 3

6

1

2 3

1

1

1 2

3

4

1

2

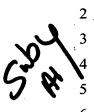
1

An apparatus comprising: 1.

an inductor having an impedance connected in series between an output of a high frequency circuit operating at a frequency and an electrostatic discharge (ESD) circuit configured to protect the high frequency circuit from an ESD event, the impedance having a substantially high value at that frequency and a substantially low value at the ESD event.

- 2. The apparatus of claim 1 wherein the ESD circuit has first and second terminals, the first terminal being connected to one end of the inductor, the second terminal being connected to ground.
- 3. The apparatus of claim 1 wherein the ESD circuit is a gate grounded 2 metal oxide semiconductor (NMOS) transistor.
  - 4. The apparatus of claim 1 wherein the ESD circuit is a diode circuit.
  - 5. The apparatus of claim 1 wherein the inductor is connected between a first bond pad of the output and a second bond pad of the ESD circuit, the first and second bond pads being on a package substrate in a package encapsulating the high frequency circuit and the ESD circuit.
  - The apparatus of claim 5 wherein the inductor is connected between the 6. first and second bond pads via first and second bond wires.
- The apparatus of claim 5 wherein the high frequency and ESD circuits 1 7. ₹2 are on a silicon die mounted on the package substrate.
- The apparatus of claim 5 wherein the package is one of a ball grid array 1 8. 2 (BGA) package and a flip-chip package.
- 1 9. The apparatus of claim 1 wherein the frequency is higher than 1 2 gigahertz.

1	10.	The apparatus of	claim 1	wherein th	e ESD e	vent co	rrespon	ds to a le	ow
2	frequency eve	ent.							
•	1.1								
I	11.	A method compri	şıng:						



1

2

3

1

2

1

1

2

3

4

1

2

3

1 2

connecting an inductor in series between an output of the high frequency circuit operating at a frequency and an electrostatic discharge (ESD) circuit configured to protect the high frequency circuit from an ESD event, the inductor having an impedance with a substantially high value at the frequency and a substantially low value at the ESD event.

- The method of claim 11 wherein connecting the inductor comprises: 12. connecting a first terminal of the ESD circuit to one end of the inductor, and connecting a second terminal of the ESD circuit to ground.
- The method of claim 11 wherein the ESD circuit is a gate grounded metal oxide semiconductor (NMOS) transistor.
  - 14. The method of claim 11 wherein the ESD circuit is a diode circuit.
- 15. The method of claim 1 wherein connecting the inductor comprises connecting the inductor between a first bond pad of the output and a second bond pad of the ESD circuit, the first and second bond pads being on a package substrate in a package encapsulating the high frequency circuit and the ESD circuit.
- 16. The method of claim 15 wherein connecting the inductor comprises connecting one end of the inductor to the first bond pad via a first bond wire; and connecting an other end of the inductor to the second bond pad via a second bond wire.
- The method of claim 15 wherein connecting the inductor comprises: 1 17. 2 mounting a silicon die containing the high frequency and ESD circuits on the 3 package substrate.
  - The method of claim 15 wherein the package is one of a ball grid array 18. (BGA) package and a flip-chip package.

U

N

П



3

4

5

6

7

8

9

1	19.	The method of claim	1 wherein the frequency is higher than 1
2	gigahertz.		

- The method of claim 11 wherein the ESD event corresponds to a low 1 20. 2 frequency event.
  - 21. A circuit comprising
  - a high frequency circuit operating at a frequency, the high frequency circuit having an output;
  - an electrostatic discharge (HSD) circuit configured to protect the high frequency circuit from an ESD event; and
  - an inductor having an impedance connected in series between the output of the high frequency circuit and the electrostatic discharge (ESD) circuit, the impedance having a substantially high value at the frequency and a substantially low value at the ESD event.
- 22. The circuit of claim 11 wherein the ESD circuit has first and second 1 2 terminals, the first terminal being connected to one end of the inductor, the second 3 terminal being connected to ground.
- 1 23. The circuit of claim 11 wherein the ESD circuit is a gate grounded metal 2. oxide semiconductor (NMOS) transistor.
- 1 24. The circuit of claim 11 wherein the ESD circuit is a diode circuit.
- 1 25. The circuit of claim 11 wherein the inductor is connected between a first 2 bond pad of the output and a second bond pad of the ESD circuit, the first and second bond pads being on a package substrate in a package encapsulating the high frequency 3 circuit and the ESD circuit.
- 1 26. The circuit of claim 15 wherein the inductor is connected between the 2 first and second bond pads via first and second bond wires.
- 27. 1 The circuit of claim 15 wherein the high frequency and ESD circuits are 2 on a silicon die mounted on the package substrate.



- 1 28. The circuit of claim 15 wherein the package is one of a ball grid array 2 (BGA) package and a flip-chip package.
  - 29. The circuit of claim 11 wherein the frequency is higher than 1 gigahertz.
- 1 30. The circuit of claim 11 wherein the ESD event corresponds to a low frequency event.